الجامعة السورية الخاصة
SYRIAN PRIVATE UNIVERSITY

كـلـيـــة هندسة الحاسوب والمعلوماتية والاتصالات
Faculty of Computer & Informatics
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Logic Circuits

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Chapter_3
Logic Gets

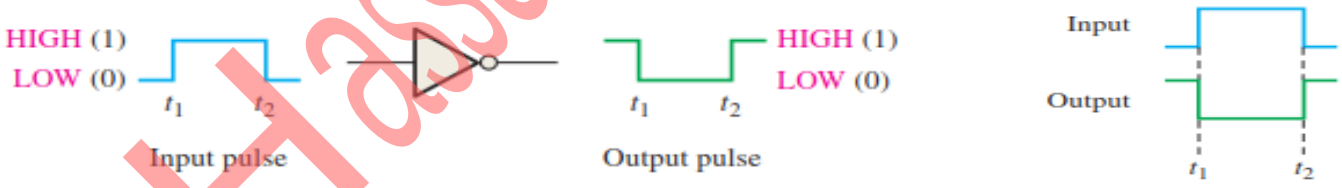
Lecture _05
Logic Gets
Operations & Truth Tables

5-1. The Inverter (العاكس)

- The **inverter** performs the Boolean **NOT** operation.

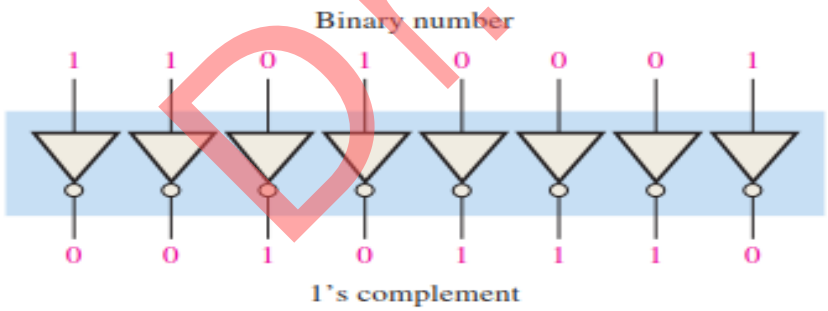
Input	Output
A	X
LOW (0)	HIGH (1)
HIGH (1)	LOW(0)

- **NOT** operation indicates inversion or complementation . Thus, the Boolean expression for an inverter is $X = \bar{A}$.
  - The complemented variable A can be read as "A bar" or "not A."
- For example, inverter operation with a pulse input, and a timing diagram:



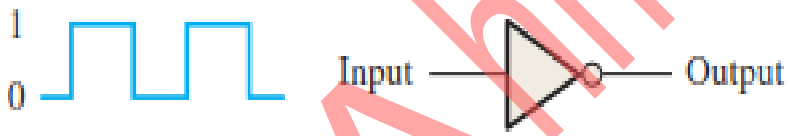
An Application

Fig. shows a circuit for producing the 1's complement of an 8-bit binary number.



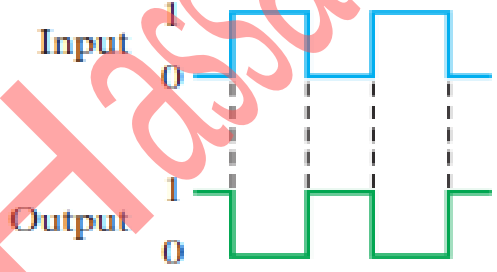
Example 5-1

A waveform is applied to an inverter in Figure. Determine the output waveform corresponding to the input and show the timing diagram. According to the placement of the bubble, what is the active output state?



Solution

The output waveform is exactly opposite to the input (inverted), as shown in Fig., which is the basic timing diagram.



5-2. The AND Gate

- The **AND gate** produces a HIGH output when all inputs are HIGH; otherwise, the output is LOW.
  - The distinctive shape (الشكل المميز) symbol

  - For a 2-input gate, the truth table is

Inputs		Output
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

1 = HIGH, 0 = LOW

AND Gate Truth Table

- The total number of possible combinations of binary inputs to a AND gate is determined by the following formula: $N = 2^n$, where N is the number of possible input combinations and n is the number of input variables.
- For example,

For two input variables: $N = 2^2 = 4$ combinations

For three input variables: $N = 2^3 = 8$ combinations

For four input variables: $N = 2^4 = 16$ combinations

Example 5-1

a) Develop the truth table for a 3-input AND gate.

b) Determine the total number of possible combinations for a 4-input AND gate.

Solution

The number of possible combinations for a 3-input AND gate is $2^3 = 8$, and the truth table is as shown.

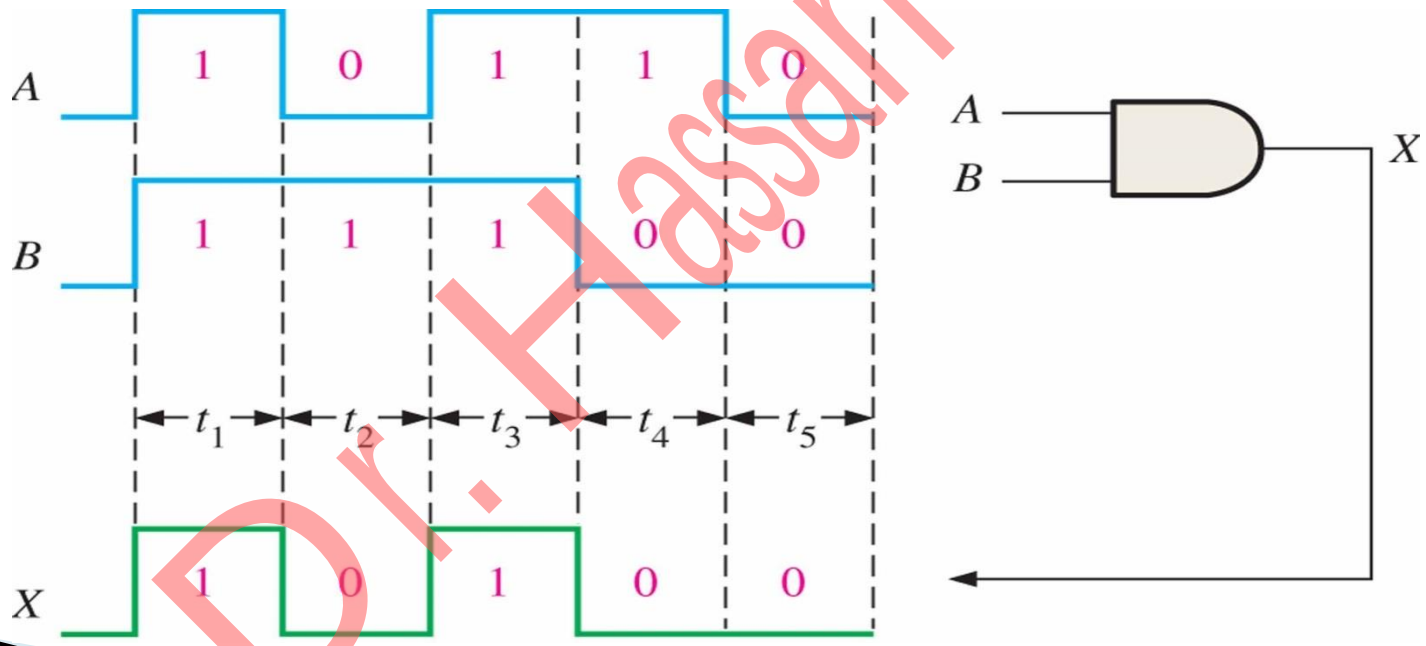
Total number: $N = 2^4 = 16$.

(There are 16 possible combinations of input bits for a 4-input AND gate)

Inputs			Output
A	*B*	*C*	*X*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

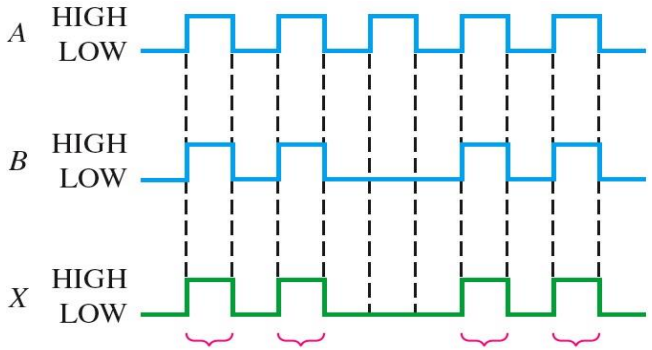
Operations with Waveform Inputs of an AND Gate

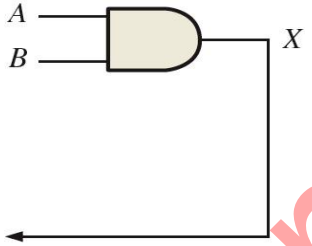
- In most applications, the inputs to a AND gate are not stationary (غير ثابتة) but are voltage waveforms that change frequency between HIGH and LOW logic levels.
- Let's look at the operation of AND gate with pulse waveform inputs, as shown in Fig.
  - As you know, a diagram of input and output waveforms showing time relationships is called ***timing diagram***.

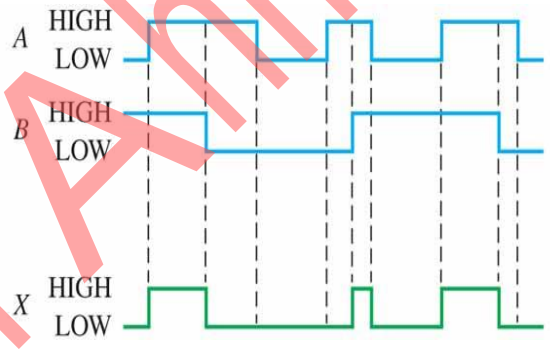


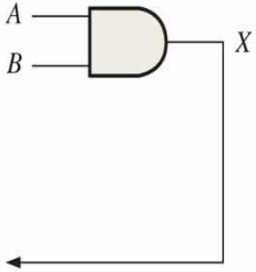
Example 5-2

If two waveforms, *A* and *B*, are applied to the AND gates inputs as shown in Fig., what is the resulting output waveform??

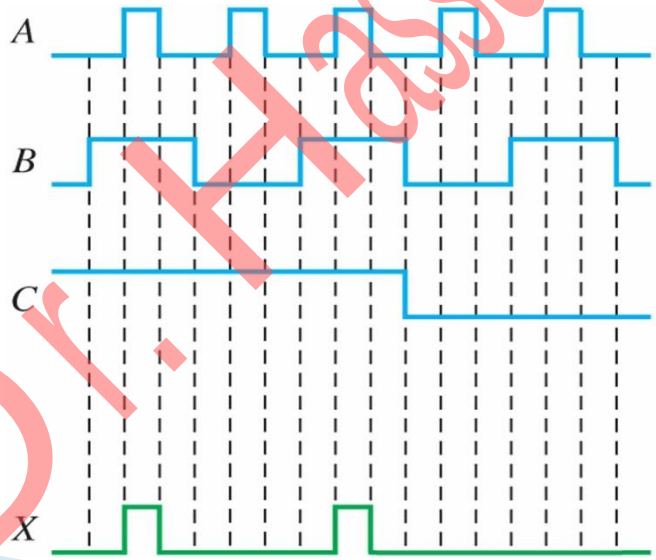


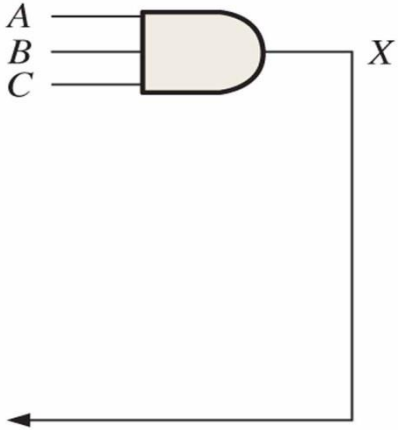






A and *B* are both HIGH during these four time intervals. Therefore *X* is HIGH.





Logic Expression for an AND Gate (التعبير المنطقي)

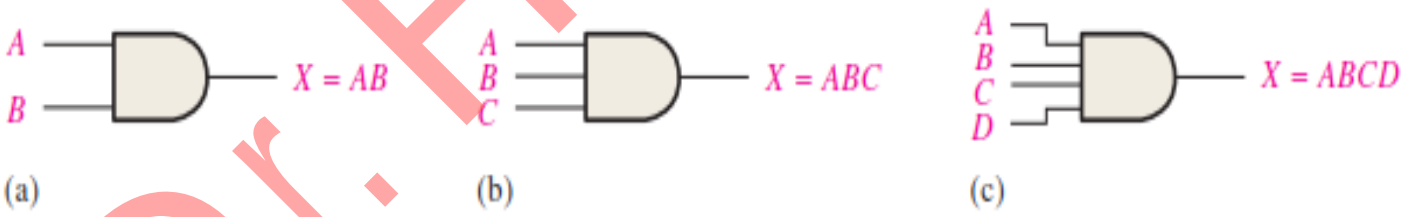
The logical AND function of two variables is represented mathematically as:

$$X = A \cdot B \text{ or } X = AB$$

Boolean Multiplication (الضرب البوليني)

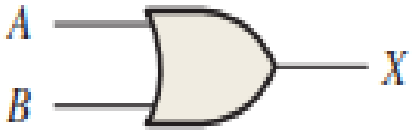
A	B	AB = X
0	0	0 · 0 = 0
0	1	0 · 1 = 0
1	0	1 · 0 = 0
1	1	1 · 1 = 1

Figure shows the AND gate logic symbol with two, three, and four inputs.



5-3. The OR Gate

- The **OR gate** produces a HIGH output if any input is HIGH; if all inputs are LOW, the output is LOW.
  - The distinctive shape (الشكل المميز) symbol



  - For a 2-input gate, the truth table is

Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	1

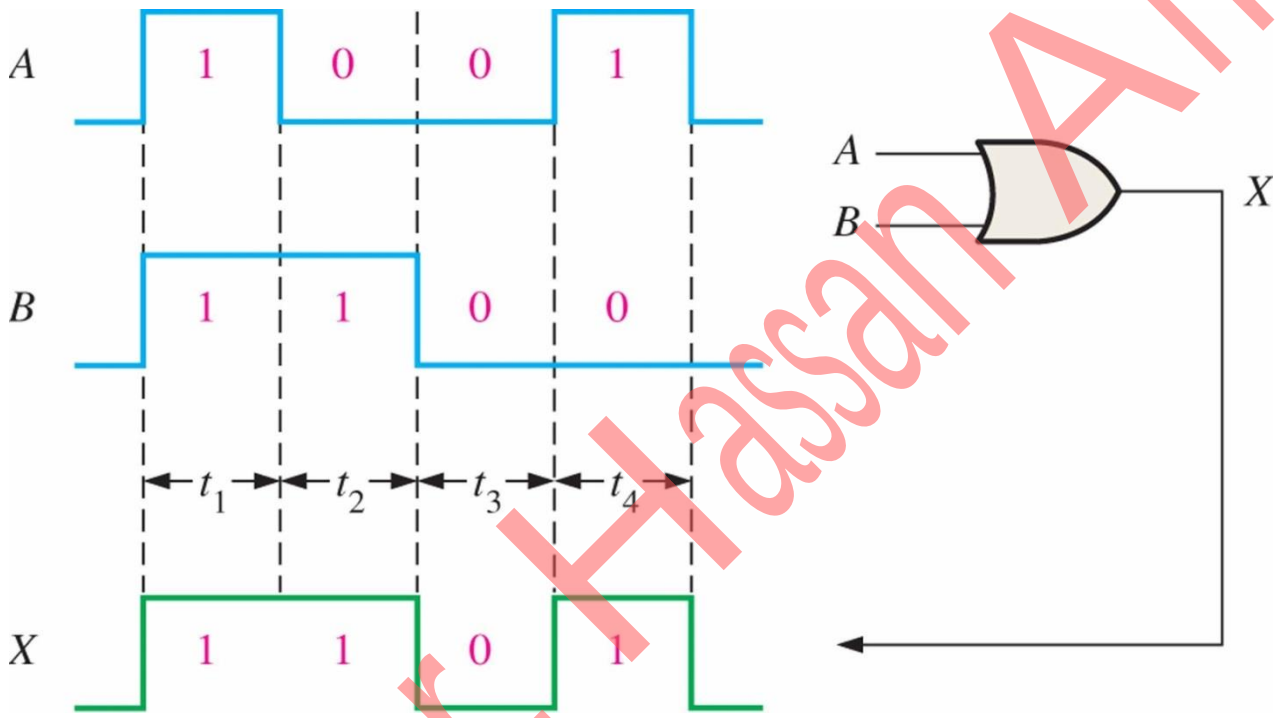
1 = HIGH, 0 = LOW

- The **OR** operation is shown with a plus sign (+) between the variables. Thus, the OR operation is written as $X = A + B$

A	*B*	*A* + *B* = *X*
0	0	0 + 0 = 0
0	1	0 + 1 = 1
1	0	1 + 0 = 1
1	1	1 + 1 = 1

Operations with Waveforms Inputs for OR Gate

Example of OR gate operation with a timing diagram showing input and output time relationships.

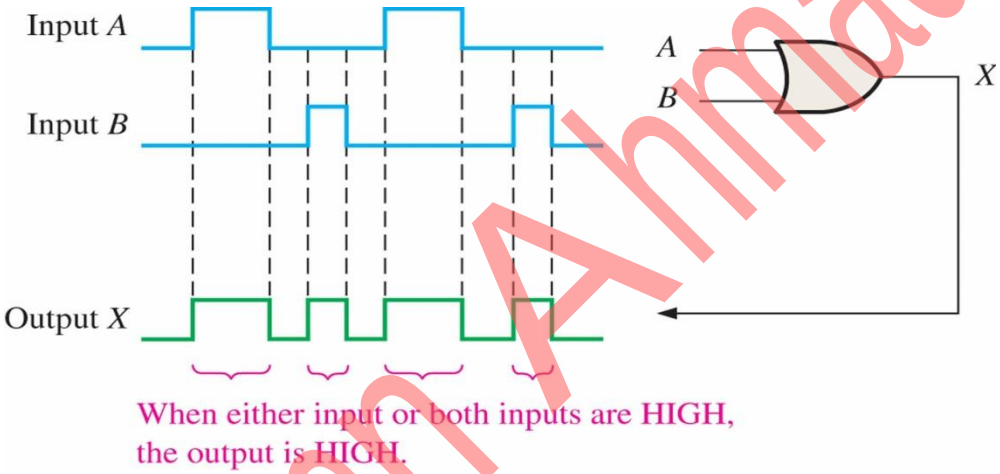


Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	1

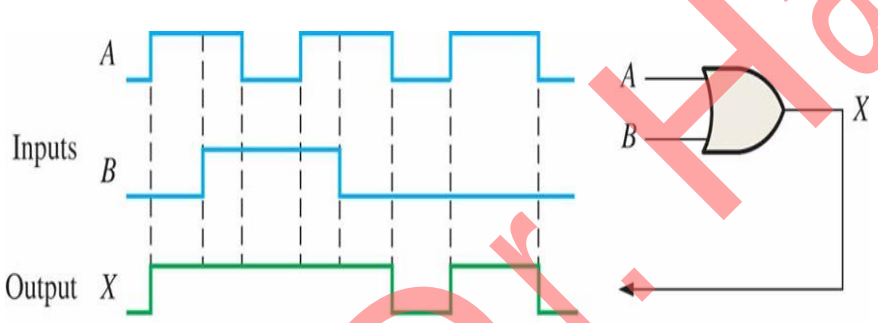
Example 5-3

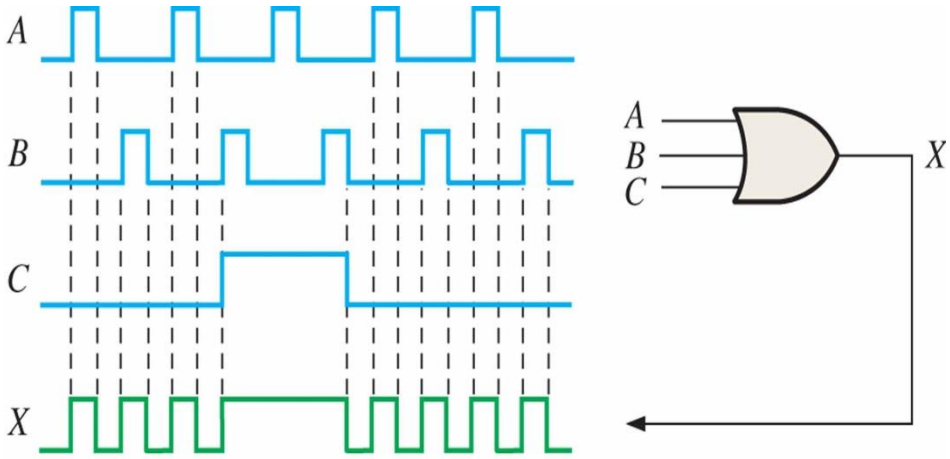
Solutions

If two input waveforms, *A* and *B*, are applied to the OR gate as shown in Fig., what is the resulting output waveform??



For the two and three input waveforms, *A* and *B*, in Fig., show the resulting output waveform with its proper relation to the inputs?





Logic Expression for an OR Gate

The logic AND function of two variables is represented mathematically as

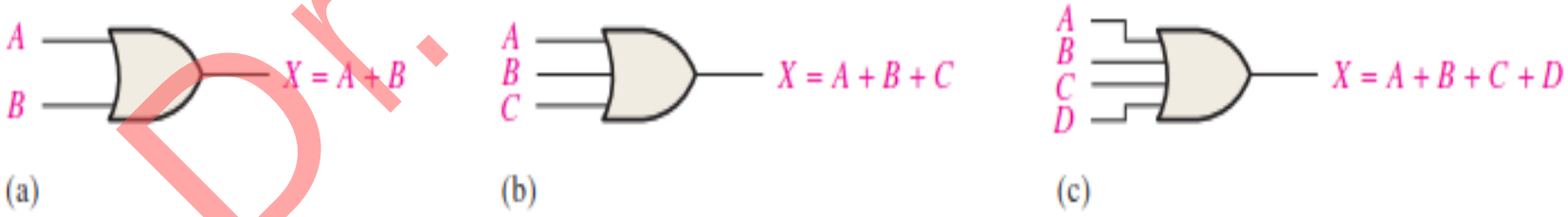
$$X = A + B$$

Boolean Addition

A	B	A + B = X
0	0	0 + 0 = 0
0	1	0 + 1 = 1
1	0	1 + 0 = 1
1	1	1 + 1 = 1

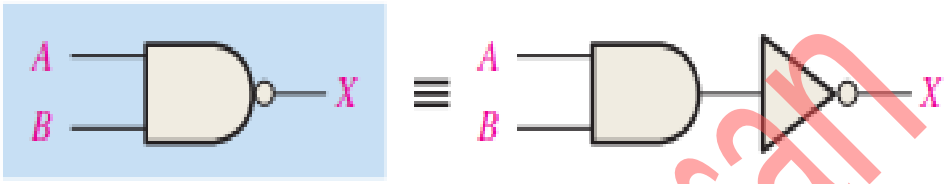
Notice that Boolean addition differs from binary addition in the case where two **1**s are added. There is **no carry** in Boolean addition.

Boolean expression for OR gates with two, three, and four inputs.



5-3. The NAND Gate

- The term **NAND** is contraction (اختصار) of NOT-AND and implies an AND function with **inverted** output.
- The **NAND gate** produces a LOW output when all inputs are HIGH; otherwise, the output is HIGH. For a 2-input gate, the truth table is



Inputs		Output
A	*B*	*X*
0	0	1
0	1	1
1	0	1
1	1	0

- The Boolean expression for the output of a 2-input NAND gate is shown with a dot between the variables and an bar over covering them. Thus, the NAND operation is written as $X = \overline{A \cdot B}$ or $X = \overline{AB}$

and all possible values of the two input variables
Are shown in Table.

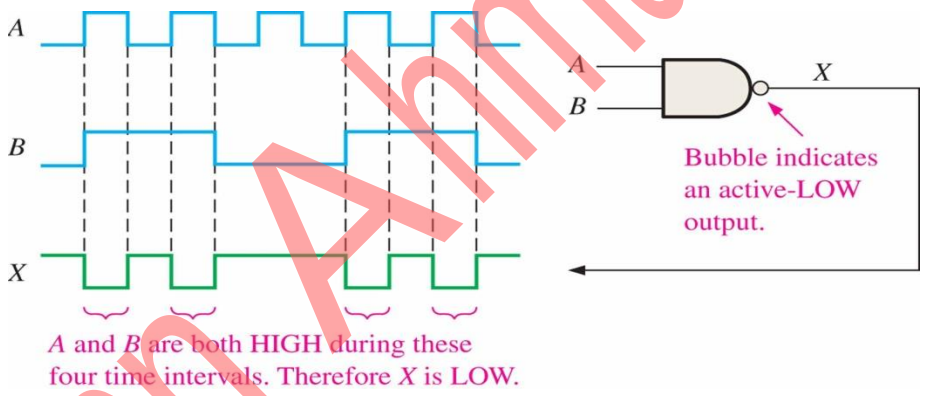
A	*B*	$\overline{AB} = X$
0	0	$\overline{0 \cdot 0} = \overline{0} = 1$
0	1	$\overline{0 \cdot 1} = \overline{0} = 1$
1	0	$\overline{1 \cdot 0} = \overline{0} = 1$
1	1	$\overline{1 \cdot 1} = \overline{1} = 0$

Operations with Waveforms Inputs for NAND Gate

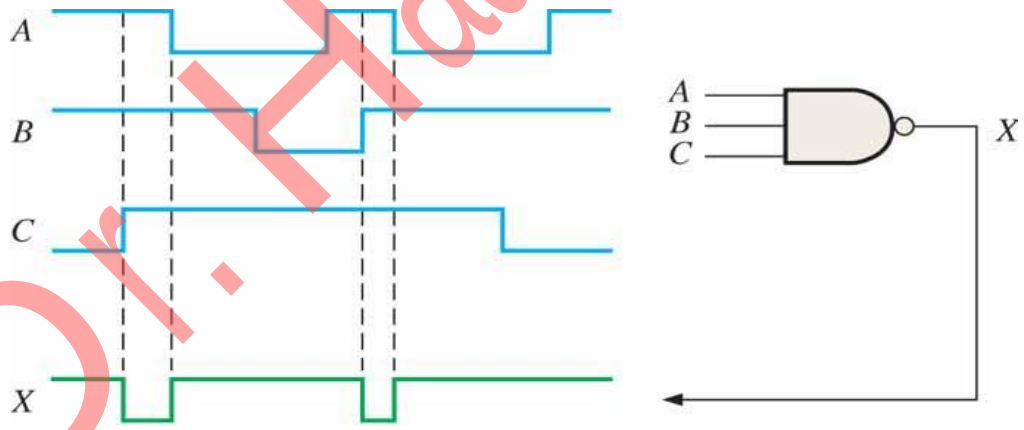
Example 5-4

Solutions

If two waveforms, *A* and *B*, are applied to the NAND gate inputs as shown in Fig., determine the resulting output waveform??

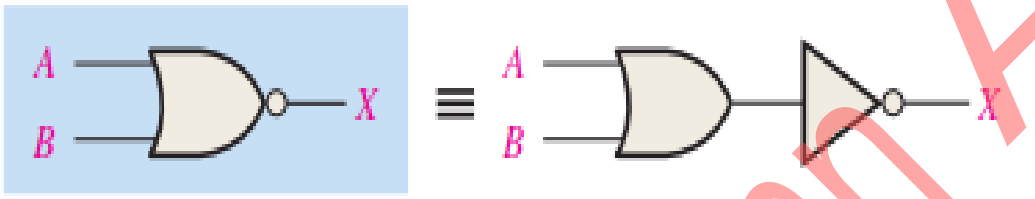


Show the resulting output waveform for 3-inputs NAND gate with its proper relation to the inputs?



5-4. The NOR Gate

- The term **NOR** is contraction of NOT-OR and implies an OR function with **inverted** output.
- The **NOR gate** produces a LOW output if any input is HIGH; if all inputs are HIGH, the output is LOW. For a 2-input gate, the truth table is



Inputs		Output
A	*B*	*X*
0	0	1
0	1	0
1	0	0
1	1	0

- The Boolean expression for the output of a 2-input NOR gate can be written as shown with a plus sign (+) between the variables and an over-bar covering them. Thus, the NOR operation is written as $X = \overline{A + B}$

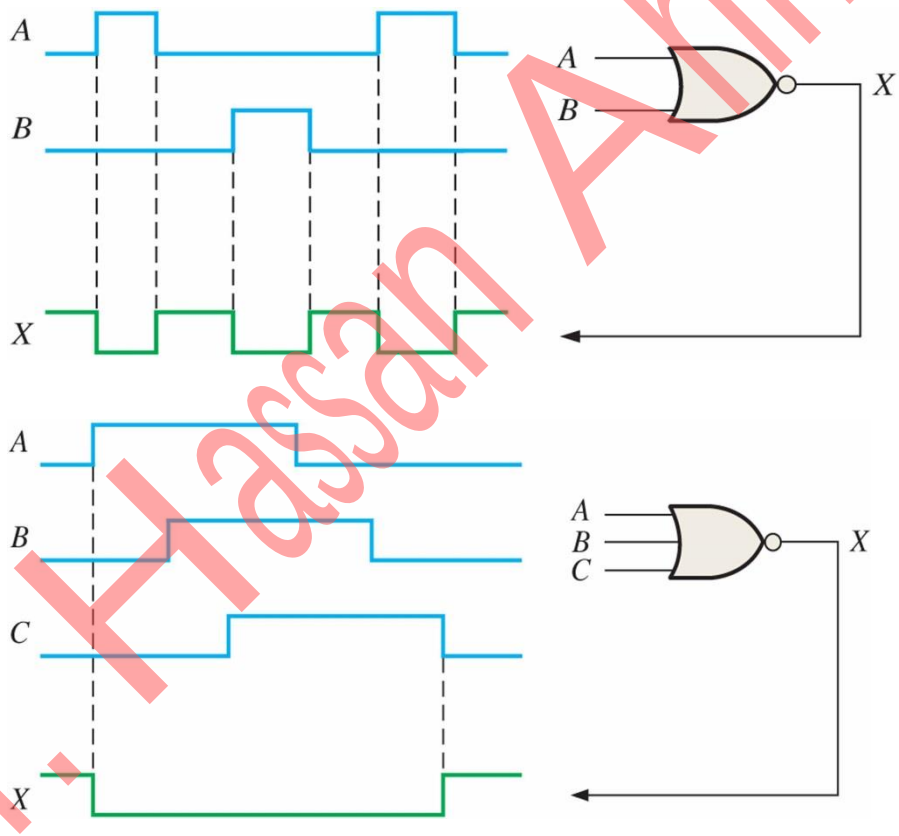
A	*B*	$\overline{A + B} = X$
0	0	$\overline{0 + 0} = \overline{0} = 1$
0	1	$\overline{0 + 1} = \overline{1} = 0$
1	0	$\overline{1 + 0} = \overline{1} = 0$
1	1	$\overline{1 + 1} = \overline{1} = 0$

Operations with Waveforms Inputs for NOR Gate

Example 5-5

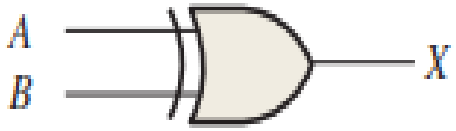
Solutions

If two (three) waveforms, *A* and *B*, (and *C*) are applied to the NOR gate inputs as in shown Fig., determine the resulting output waveform??



5-5. The Exclusive-OR Gate

- The **Exclusive-OR (XOR** for short) produces a HIGH output only when both inputs are at opposite logic levels. The truth table is

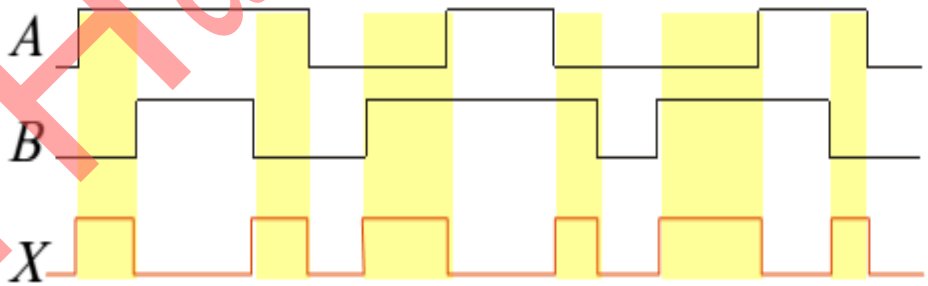


Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

- The **XOR** operation is written logically as

$$X = \overline{A}B + A\overline{B}$$

- **Example waveforms**:



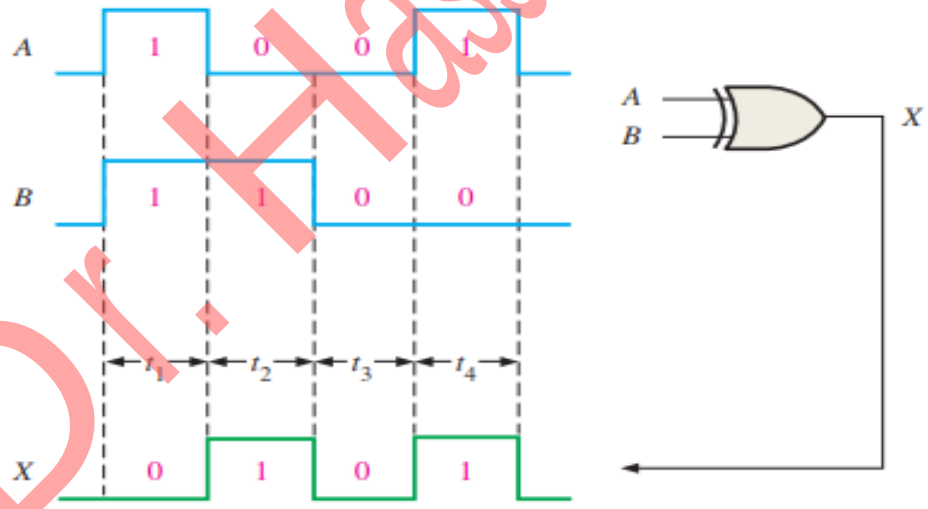
- Notice that the XOR gate will produce a HIGH only when exactly one input is HIGH.

5-6. The Exclusive-NOR Gate

- The **Exclusive-NOR gate (XNOR)** produces a HIGH output only when both inputs are at the same logic level. The truth table is

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

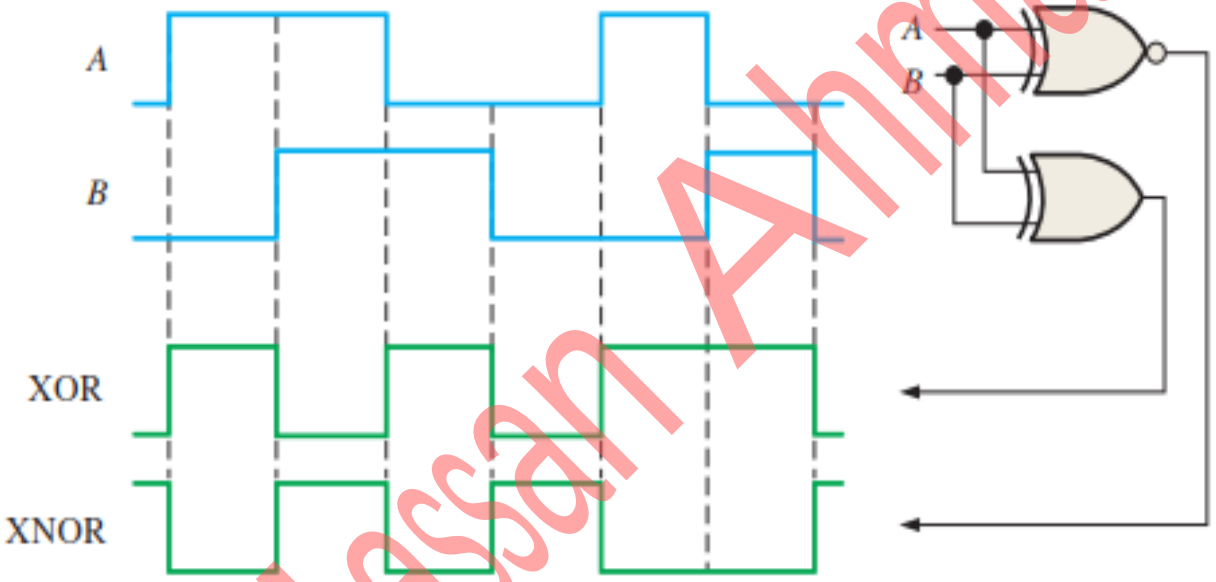
- The **XOR** operation shown as $X = \overline{A} \cdot \overline{B} + A \cdot B$
- **Example** of exclusive-OR gate operation with pulse waveform inputs.



Example 5-6

Determine the output waveforms for the XOR gate and for the XNOR gate, given the input waveforms, *A* and *B*, in Fig.

Solutions



The output waveforms are shown in Fig.

Notice that the XOR output is HIGH only when both inputs are at opposite levels.

Notice that the XNOR output is HIGH only when both inputs are the same.

Selected Key Terms

AND gate	A logic gate that produces a HIGH output only when all of the inputs are HIGH.
Boolean algebra	The mathematics of logic circuits.
Complement	The inverse or opposite of a number. LOW is the complement of HIGH, and 0 is the complement of 1.
Exclusive-NOR (XNOR) gate	A logic gate that produces a LOW only when the two inputs are at opposite levels.
Exclusive-OR (XOR) gate	A logic gate that produces a HIGH output only when its two inputs are at opposite levels.
Inverter	A logic circuit that inverts or complements its input.
NAND gate	A logic gate that produces a LOW output only when all the inputs are HIGH.
NOR gate	A logic gate in which the output is LOW when one or more of the inputs are HIGH.
OR gate	A logic gate that produces a HIGH output when one or more inputs are HIGH.
Truth table	A table showing the inputs and corresponding output(s) of a logic circuit.

True/False Quiz

1. An inverter performs a NOT operation.
2. A NOT gate cannot have more than one input.
3. If any input to an OR gate is zero, the output is zero.
4. If all inputs to an AND gate are 1, the output is 0.
5. A NAND gate can be considered as an AND gate followed by a NOT gate.
6. A NOR gate can be considered as an OR gate followed by an inverter.
7. The output of an exclusive-OR is 0 if the inputs are opposite.

1. T **2.** T **3.** F **4.** F **5.** T **6.** T **7.** F

SELF-TEST

1. When the input to an inverter is LOW (0), the output is
(a) HIGH or 0 **(b)** LOW or 0 **(c)** HIGH or 1 **(d)** LOW or 1

2. An inverter performs an operation known as
(a) complementation **(b)** assertion **(c)** inversion **(d)** both answers (a) and (c)

3. The output of an AND gate with inputs A, B and C is 0 (LOW) when
(a) $A = 0, B = 0, C = 0$ **(b)** $A = 0, B = 1, C = 1$ **(c)** both answers (a) and (b)

4. The output of an OR gate with inputs A, B and C is 0 (LOW) when
(a) $A = 0, B = 0, C = 0$ **(b)** $A = 0, B = 1, C = 1$ **(c)** both answers (a) and (b)

5. A pulse is applied to each input of a 2-input NAND gate. One pulse goes HIGH at $t = 0$ and goes back LOW at $t = 1$ ms. The other pulse goes HIGH at $t = 0.8$ ms and goes back LOW at $t = 3$ ms. The output pulse can be described as follows:
(a) It goes LOW at $t = 0$ and back HIGH at $t = 3$ ms.
(b) It goes LOW at $t = 0.8$ ms and back HIGH at $t = 3$ ms.
(c) It goes LOW at $t = 0.8$ ms and back HIGH at $t = 1$ ms.
(d) It goes LOW at $t = 0.8$ ms and back LOW at $t = 1$ ms.

6. A pulse is applied to each input of a 2-input NOR gate. One pulse goes HIGH at $t = 0$ and goes back LOW at $t = 1$ ms. The other pulse goes HIGH at $t = 0.8$ ms and goes back LOW at $t = 3$ ms. The output pulse can be described as follows:
(a) It goes LOW at $t = 0$ and back HIGH at $t = 3$ ms.
(b) It goes LOW at $t = 0.8$ ms and back HIGH at $t = 3$ ms.
(c) It goes LOW at $t = 0.8$ ms and back HIGH at $t = 1$ ms.
(d) It goes HIGH at $t = 0.8$ ms and back LOW at $t = 1$ ms.

1. (c) **2.** (d) **3.** (c) **4.** (a) **5.** (c) **6.** (a) **7.** (d) **8.** (b)

SELF-TEST

7. A pulse is applied to each input of an exclusive-OR gate. One pulse goes HIGH at $t = 0$ and goes back LOW at $t = 1$ ms. The other pulse goes HIGH at $t = 0.8$ ms and goes back LOW at $t = 3$ ms. The output pulse can be described as follows:

(a) It goes HIGH at $t = 0$ and back LOW at $t = 3$ ms.
(b) It goes HIGH at $t = 0$ and back LOW at $t = 0.8$ ms.
(c) It goes HIGH at $t = 1$ ms and back LOW at $t = 3$ ms.
(d) both answers (b) and (c)

8. A positive-going pulse is applied to an inverter. The time interval from the leading edge of the input to the leading edge of the output is 7 ns. This parameter is

(a) speed-power product
(b) propagation delay, t_{PHL}
(c) propagation delay, t_{PLH}
(d) pulse width

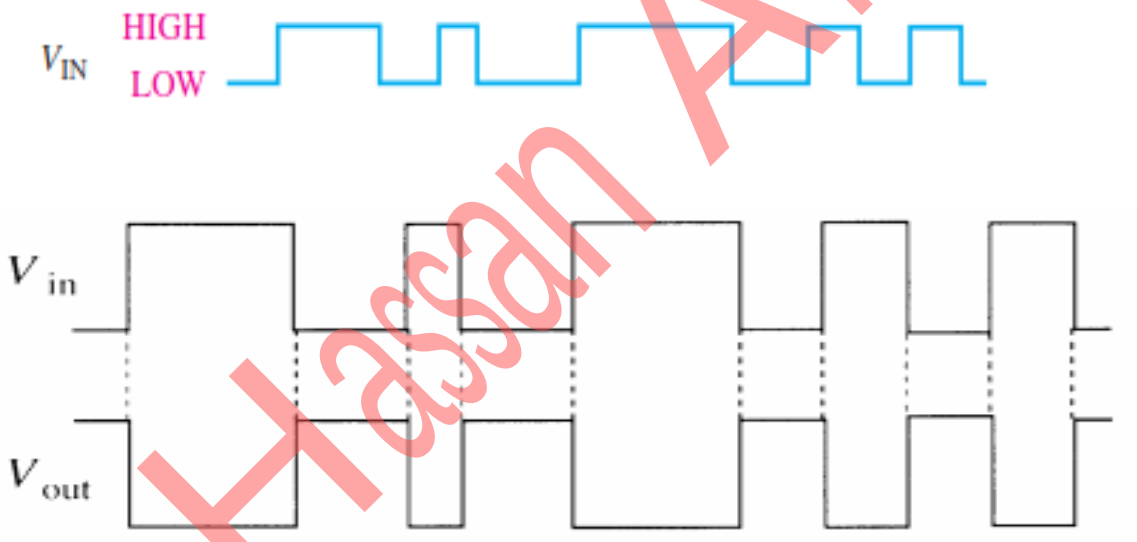
- t_{PHL}: The time between a specified reference point on the input pulse and a corresponding reference point on the resulting output pulse, with the output changing from the HIGH level to the LOW level (HL).
- t_{PLH}: The time between a specified reference point on the input pulse and a corresponding reference point on the resulting output pulse, with the output changing from the LOW level to the HIGH level (LH).

1. (c) **2.** (d) **3.** (c) **4.** (a) **5.** (c) **6.** (a) **7.** (d) **8.** (b)

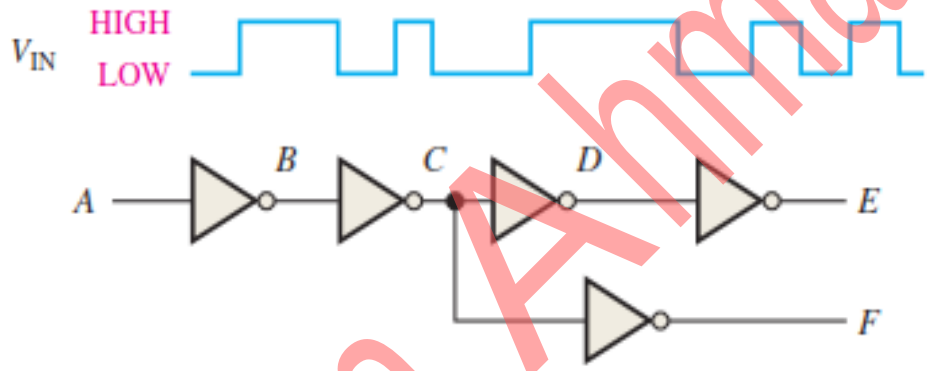
Problems & Solutions

Prob. 3-1 The input waveform shown in Fig. is applied to an inverter. Draw the output waveform in proper relation to the input.

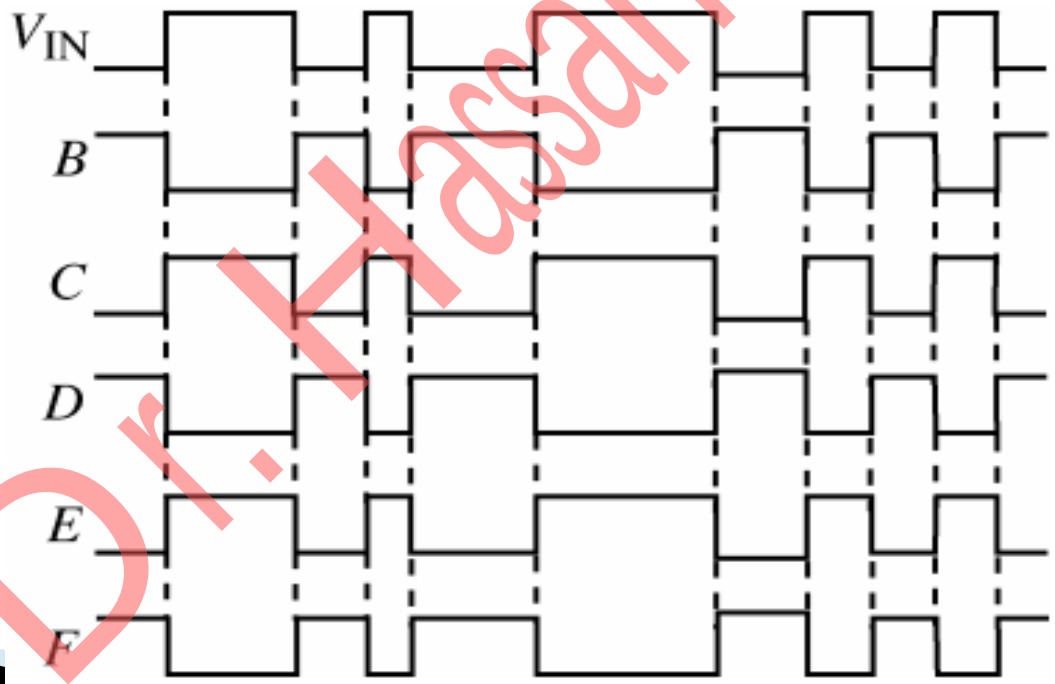
Sol.



Prob. 3-2 If the waveform in Fig. is applied to point *A* of combination of inverters shown in Fig., determine the waveforms at points *B* through *F*.

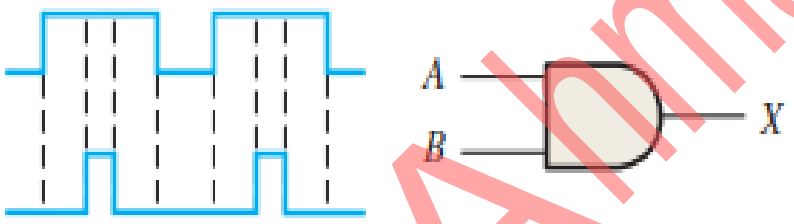


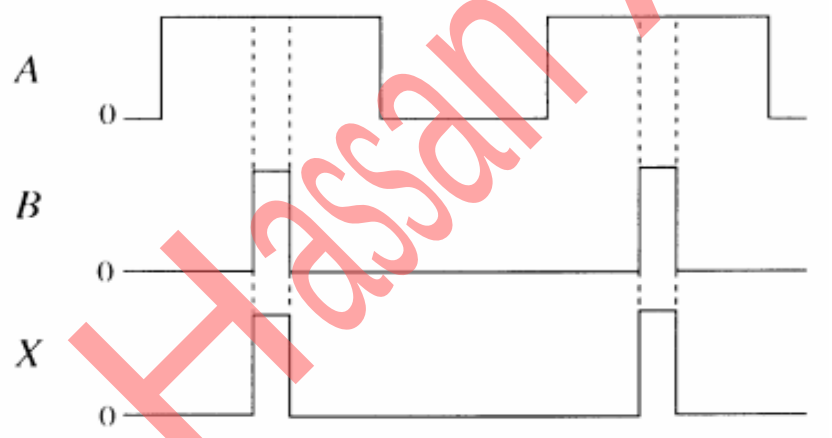
Sol.



Prob. 3-3 Determine the output, X, for a 2-input AND gate with the input waveforms shown in Fig. Show the proper relationship of output to inputs with a timing diagram.

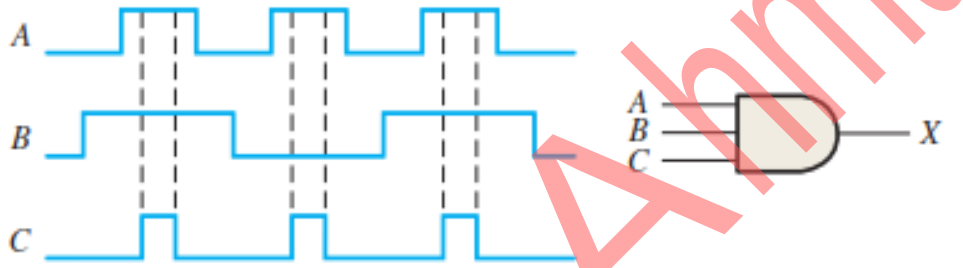
Sol.

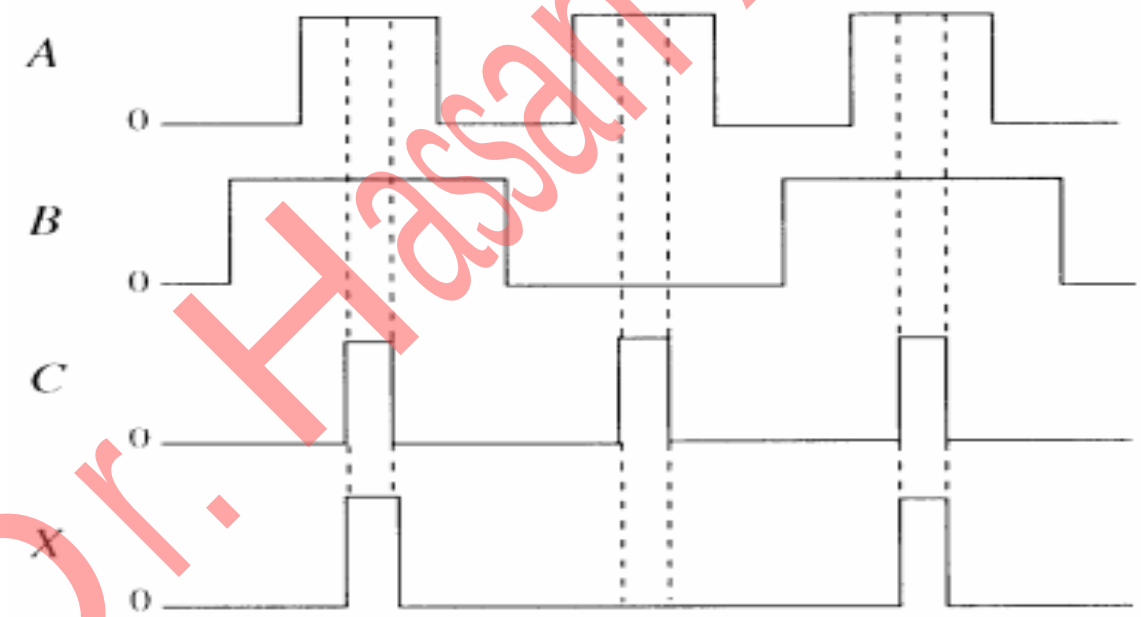




Prob. 3-4 The input waveforms applied to a 3-input AND gate are as indicated in Fig. Show the output waveform in proper relation to the inputs with a timing diagram.

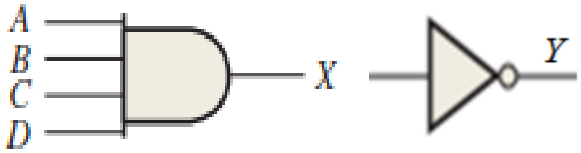
Sol.



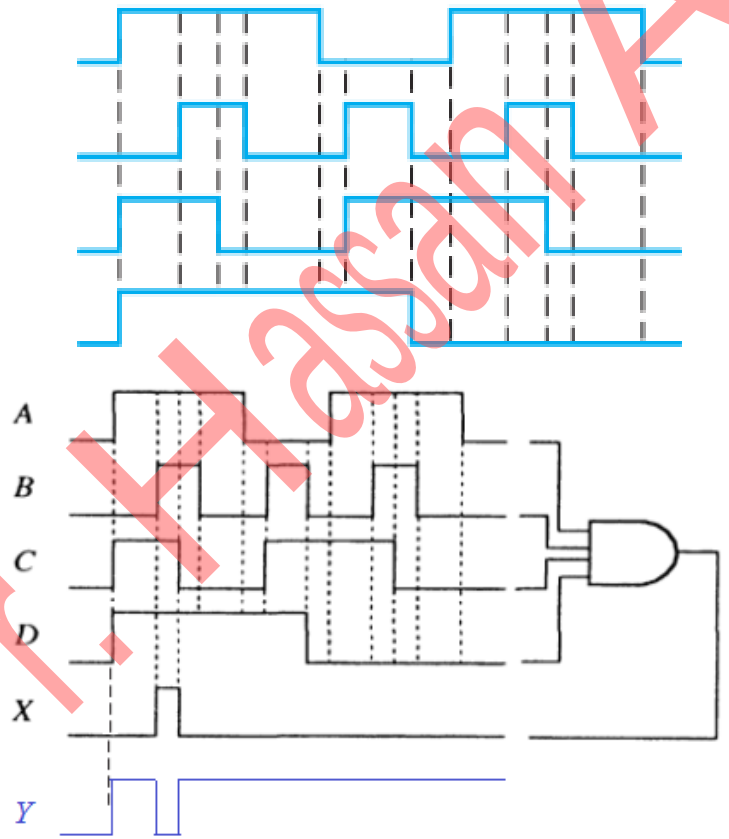


Prob. 3-5 The input waveforms applied to a 4-input AND gate are as indicated in Fig.

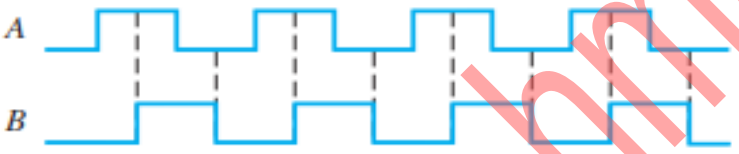
1) Show the output waveform in proper relation to the inputs with timing diagram.
2) If the output of the AND gate is fed to an inverter, draw the net output waveform (Y) of this system.



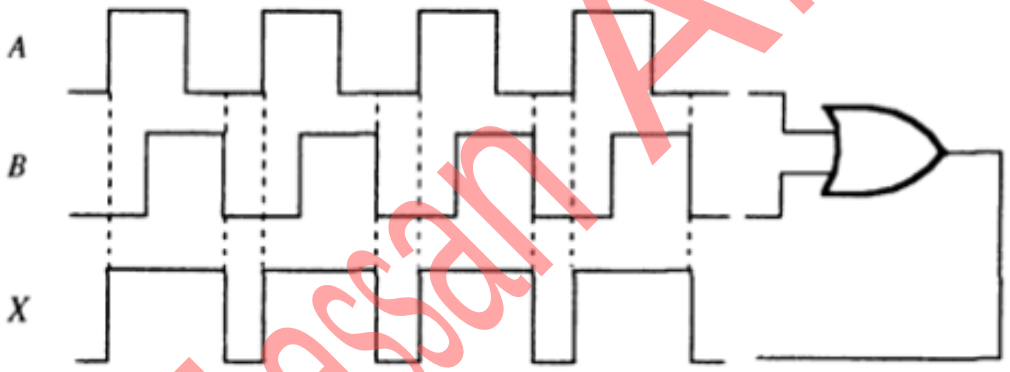
Sol.



Prob. 3-6 Determine the output for a 2-input OR gate when the input waveforms are as shown in Fig. and draw a timing diagram.

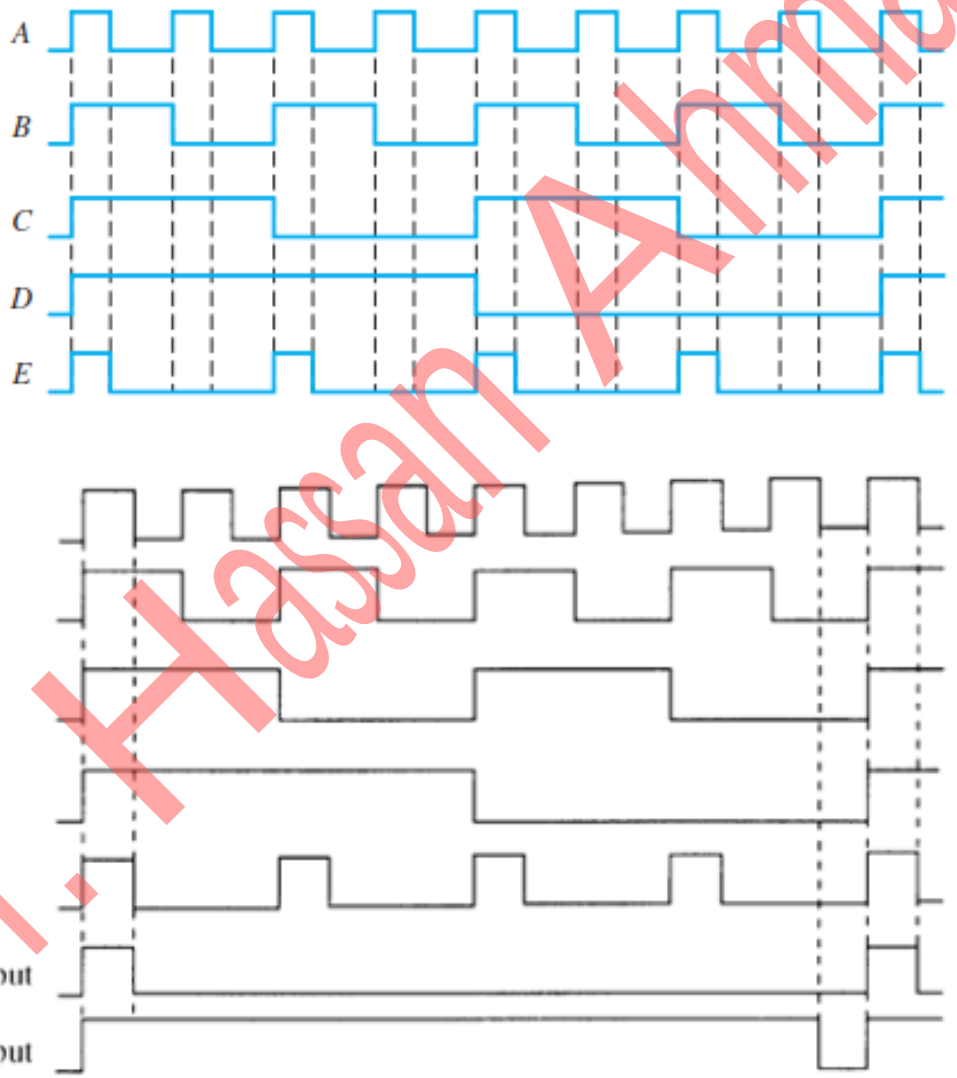


Sol.



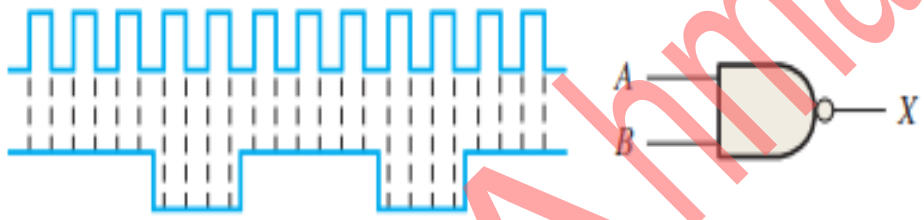
Prob. 3-7 For the five input waveforms in Fig., determine the output for a 5-input AND gate and the output for a 5-input OR gate. Draw the timing diagram.

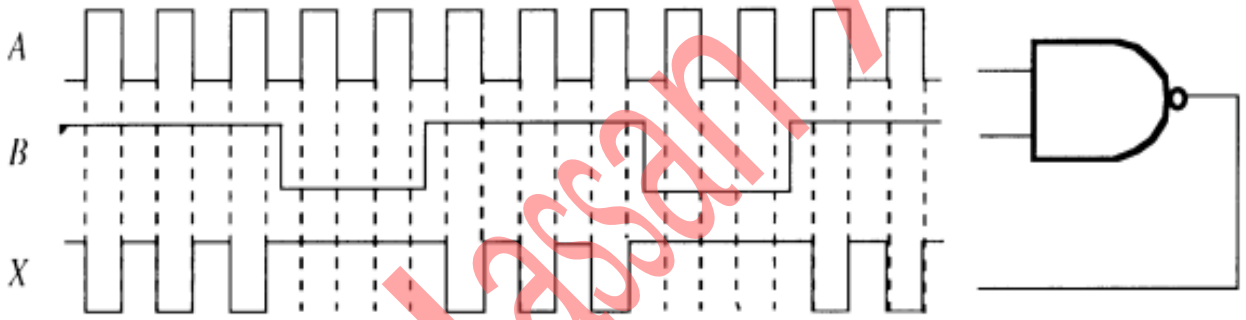
Sol.



Prob. 3-8 For the set of input waveforms in Fig., determine the output for the NAND Gate shown and draw the timing diagram.

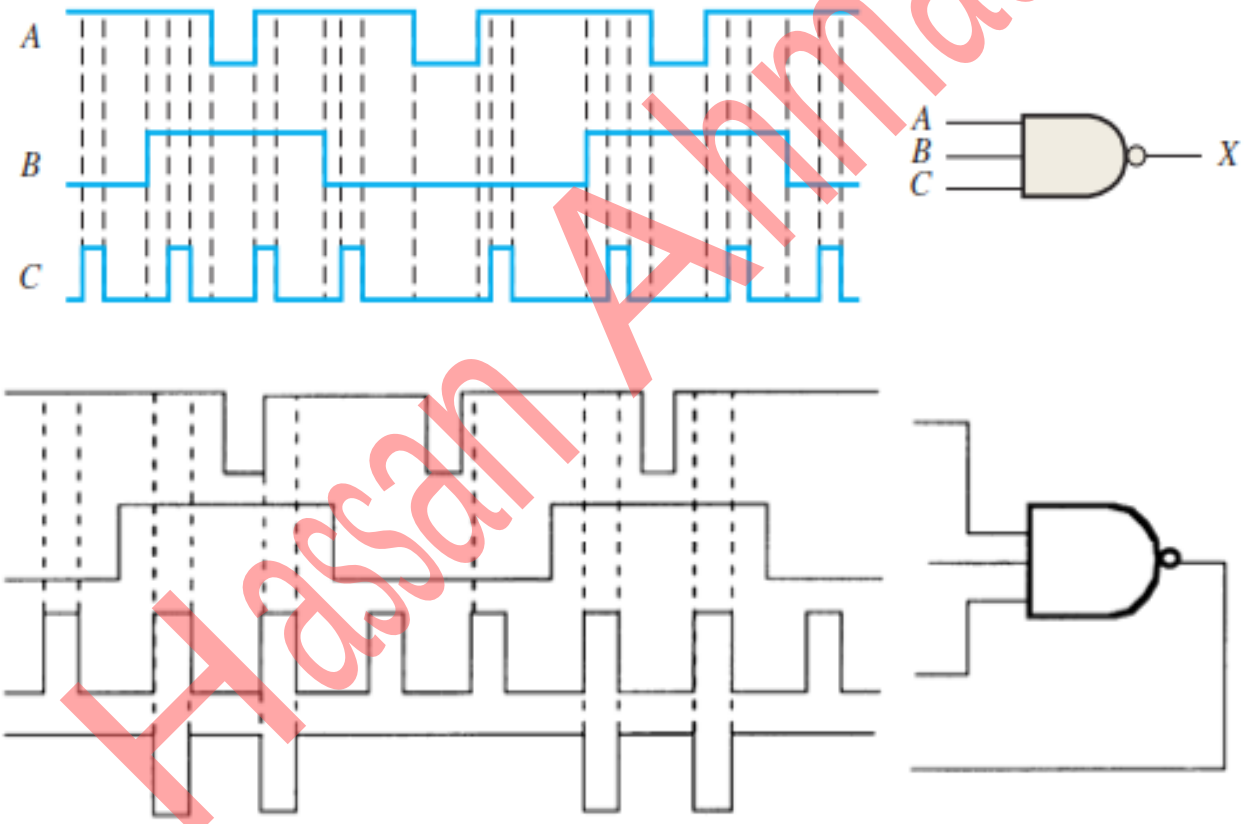
Sol.





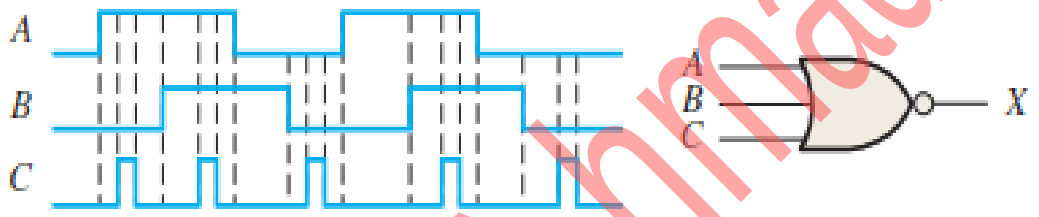
Prob. 3-9 Determine the gate output for the input waveforms in Fig. and draw the timing diagram.

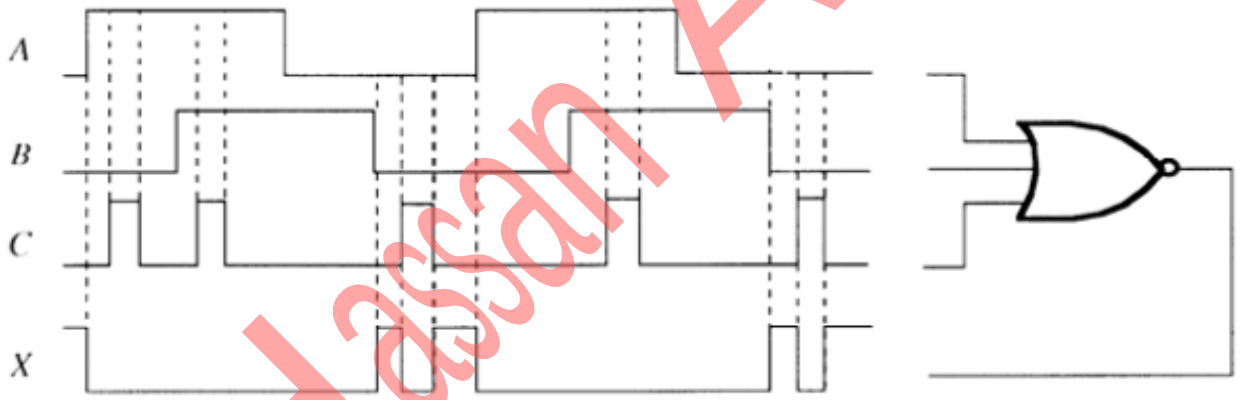
Sol.



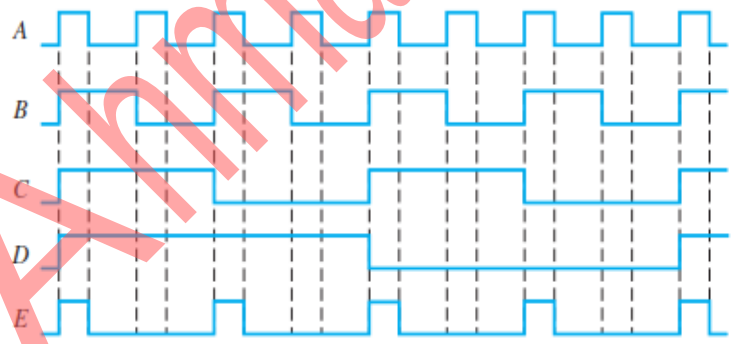
Prob. 3-9 Determine the output waveform in Fig. and draw the timing diagram.

Sol.

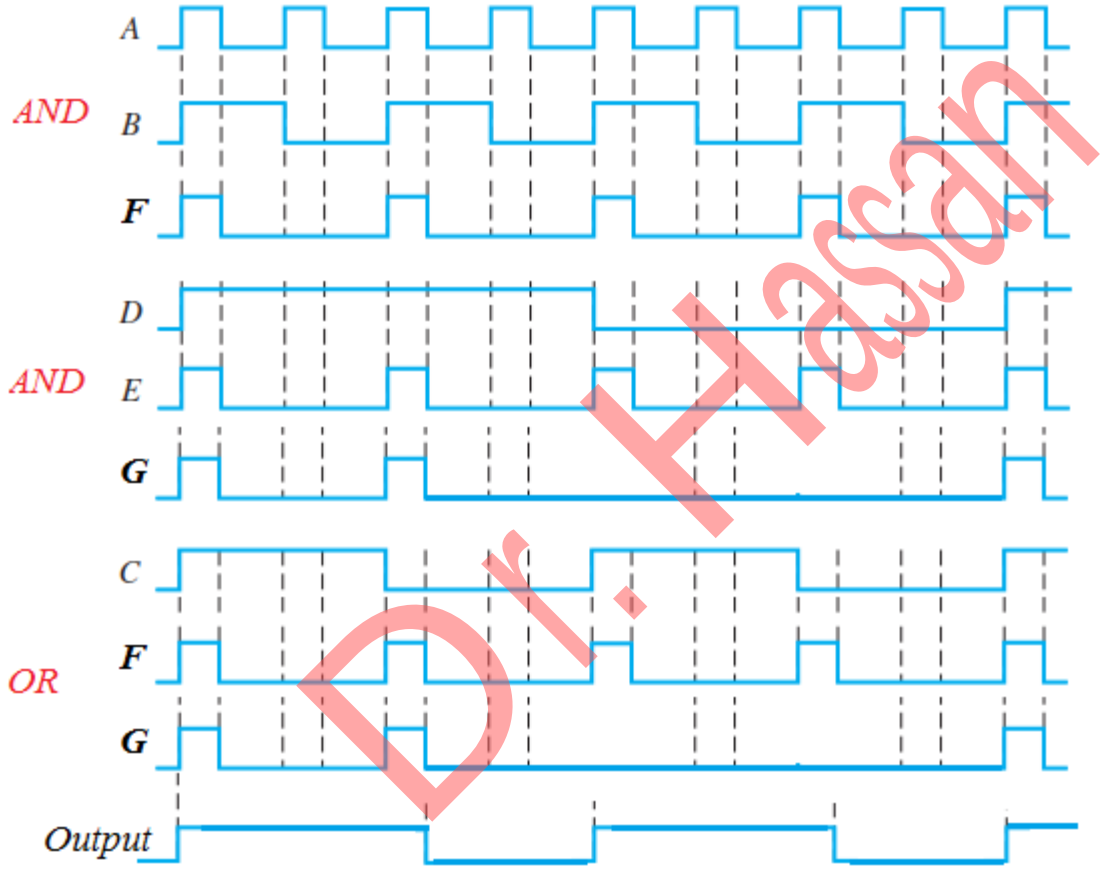




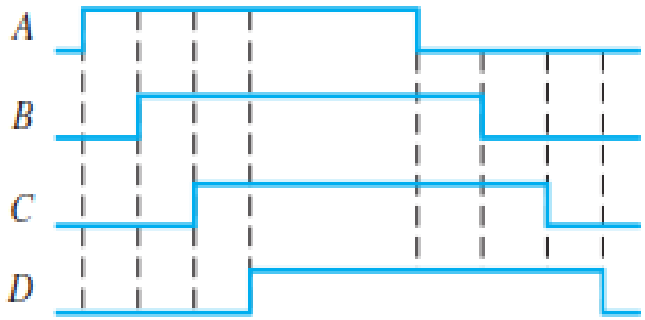
Prob. 3-10 For the waveforms given in Fig., *A* and *B* are ANDed with output *F*, *D* and *E* are ANDed with output *G*, and *C*, *F*, and *G* are ORed. Draw the net output waveform.

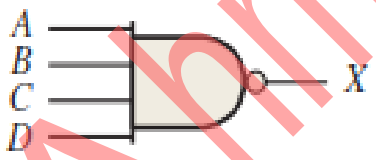


Sol.

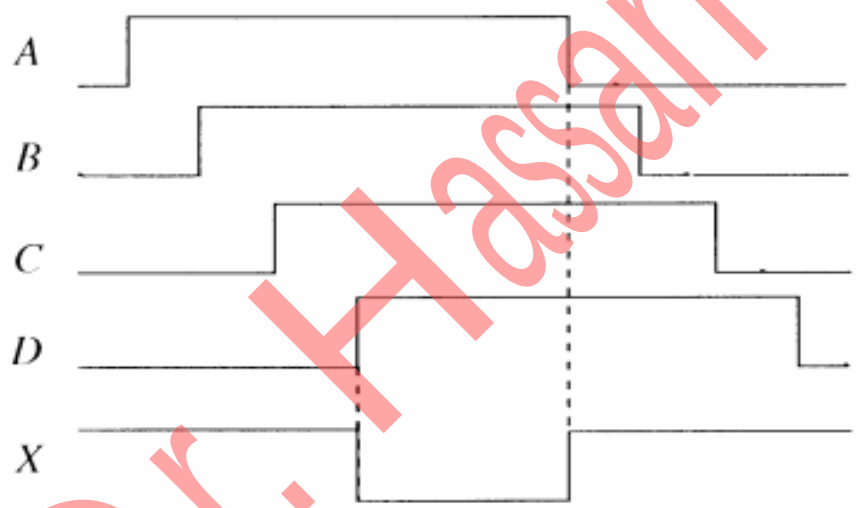


Prob. 3-11 Determine the output waveform in Fig.





Sol.



The end of Lecture_05, chapter 3